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END920030091US1

SERIAL NO. 10/721561

Krishnendu Mondal et al.

FILING 11/25/2003

GROUP 2863

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TL	6,574,757	6/2003	Park et al.	714	710	
TL	6,560,740	5/2003	Zuraski, Jr. et al.	714	733	
TL	6,505,324	1/2003	Cowan et al.	716	4	
TL	6,469,949	10/2002	Hsu et al.	365	225.7	
TL	6,408,401	6/2002	Bhavsar et al.	714	7	
TL	6,405,331	6/2002	Chien	714	718	
TL	6,367,042	4/2002	Phan et al.	714	733	
TL	6,182,257	1/2001	Gillingham	714	733	
TL	6,141,267	10/2000	Kirihata et al.	365	200	
TL	6,073,258	6/2000	Wheater	714	718	
TL	5,841,784	11/1998	Chan et al.	714	718	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TL		Barth et al., METHOD TO REDUCE CHIP YIELD LOSS DUE TO FUSES INCORRECTLY BLOWN, Research Disclosure, May 1990, Number 313, 1 page.
TL		IBM Technical Disclosure Bulletin R. J. Prilik, Vol. 30, No. 11, April 1988, REPAIR CALCULATION FOR RANDOM-ACCESS MEMORY REDUNDANCY USING BUILT-IN LOGIC AND SCANNABLE LATCHES, pages 424-425.

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TL	5,805,789	9/1998	Huott et al.	714	7	
TL	5,764,878	6/1998	Kablanian et al.	714	7	
TL	5,659,551	8/1997	Huott et al.	714	725	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
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